What is claimed is:

1. A fabrication method for flash memory, comprising:

providing a substrate, wherein a plurality of device isolation regions are formed on the substrate to define a plurality of striped active areas;

forming a deep well of first conductive type in the substrate, wherein the deep well of first conductive type contains the active areas and the area below the device isolation regions;

forming a tunneling oxide layer and a first electrically conductive layer on the active area;

forming a dielectric layer on the substrate on which the first electrically conductive layer is formed;

forming a second electrically conductive layer on the dielectric layer;

defining the second electrically conductive layer, the dielectric layer and the first electrically conductive layer, so as to convert the second electrically conductive layer and the first electrically conductive layer into a plurality of stacked gate structures composed of a plurality of control gates and a plurality of floating gates;

forming a plurality of wells of second conductive type in an area disposed between the adjacent control gates in the substrate, wherein the plurality of wells of second conductive type contain the area disposed below the device isolation regions;

forming a plurality of drains in the active areas located on one side of the control gates, wherein the drains are enclosed by the wells of second conductive type;

forming a plurality of spacers on both sides of the stacked gate structures; and

forming a plurality of sources in the active areas located on the other side of the control gates, wherein the sources are

located on both sides of the wells of second conductive type and electrically connected with each other via the deep well of first conductive type.

2. The fabrication method of claim 1, wherein the device isolation regions are field oxide layers.

3. The fabrication method of claim 1, wherein the device isolation region is shallow trench isolations.

4. The fabrication method of claim 1, wherein the deep well of first conductive type is a deep n-type doped well; the wells of second conductive type are p-type doped wells; the sources are n-doped regions; and the drains are n-type doped regions.

5. The fabrication method of claim 4, wherein the method to form the deep well of first conductive type comprises the steps of:

forming a photoresist layer on the substrate, wherein a pattern of the deep well of first conductive type is defined on the photoresist layer;

performing an ion implantation; and

removing the photoresist layer.

6. The fabrication method of claim 5, wherein the ion implantation comprises two stages, and the first stage implants phosphorous ions of about 5×10^{13} ~$1\times10^{14}/cm^2$ at about 800keV to about 1.5MeV, and the second stage implants phosphorous ions of about $1\times10^{13}/cm^2$ at about 360keV.

7. The fabrication method of claim 1, wherein, before the tunneling oxide layer is formed on the active regions, the fabrication method further comprises the steps of:

forming a photoresist layer on the substrate, wherein a pattern of a plurality of flash memory cells is defined on the photoresist layer;

performing an ion implantation to adjust the threshold voltage of the flash memory; and

removing the photoresist layer.

8. The fabrication method of claim 7, wherein the ion implantation is performed to implant boron ions of about 5×10^{11} ~ $1\times10^{12}/cm^2$ at about 60keV.

9. The fabrication method of claim 1, wherein the dielectric layer located between the control gates and the floating gates is a stacked structure of silicon oxide/silicon nitride/silicon oxide.

10. The fabrication method of claim 1, wherein the method to form the wells of second conductive type comprises the steps of:

forming a photoresist layer on the substrate to define a pattern of the area located between the control gates corresponding to the drain;

performing an ion implantation;

removing the photoresist layer; and

performing a heat treatment.

11. The fabrication method of claim 10, wherein the ion implantation is performed to implant boron ions of about 5×10^{12} ~ $1\times10^{13}/cm^2$ at about 60keV.

12. The fabrication method of claim 10, wherein the heat treatment is performed for about 25 ~ 35 minutes in an oxygen (O_2) environment of about 900 ℃, so as to extend the wells of

second conductive type to a striped type, and the striped wells of second conductive type being parallel to the control gates.

13. The fabrication method of claim 1, wherein the sources and the drains are formed by implanting arsenic (As) of about 1.5×10^{15} ~ $2\times10^{15}/cm^2$ at about 50keV.

14. The fabrication method of claim 1, further comprising the steps of:

forming an interlayer dielectric layer on the substrate on which the sources and the drains are formed;

forming a plurality of contact plugs connecting to the drains in the interlayer dielectric layer; and

forming a plurality of wordlines on the interlayer dielectric layer in which the contact plugs are formed.

15. A structure of flash memory, comprising:

a plurality of device isolation regions located in a substrate to define a plurality of active areas;

a deep well of first conductive type located in the substrate, wherein the deep well of first conductive type contains the active area and the area below the device isolation regions;

a plurality of stacked gate structures located on the substrate, wherein the stacked gate structures are composed of a plurality of floating gates, a dielectric layer and a plurality of control gates;

a tunneling oxide layer located between the stacked gate structures and the substrate;

a plurality of wells of second conductive type located in an area disposed between the adjacent control gates in the substrate, wherein the plurality of wells of second conductive type contain the area disposed below the device isolation regions;

a plurality of spacers located on both sides of the stacked gate structures; and

a plurality of sources and a plurality of drains, wherein the sources and the drains are located in the active area located on both sides of the control gates, and the drains are enclosed by the wells of second conductive type, and the sources are located on both sides of the wells of second conductive type, and the sources are electrically connected with each other via the deep well of first conductive type.

16. The structure of flash memory of claim 15, wherein the device isolation regions are field oxide layers.

17. The structure of flash memory of claim 15, wherein the device isolation regions are shallow trench isolations.

18. The structure of flash memory of claim 15, wherein the deep well of first conductive type is an n-type doped well region; the wells of second conductive type are p-type doped wells; the sources are n-type doped regions; and the drains are n-type doped regions.

19. The structure of flash memory of claim 15, wherein the dielectric layer located between the control gate and the floating gate is a stacked structure of silicon oxide/silicon nitride/silicon oxide.

20. The structure of flash memory of claim 15, further comprising:

a plurality of contact plugs located on the drains and electrically connected to the drains; and

a plurality of bitlines electrically connected to the drains via the contact plugs.

21. An operating method to erase, programming and reading data on a flash memory, wherein a wordline voltage, a bitline voltage and a p-type doped well voltage are respectively applied to a control gate, a drain and a p-type doped well, all of which correspond to a selected flash memory cell; a source of the flash memory is a common source, and electrically connected via a deep n-type doped well; the drain is commonly used by the selected flash memory cell and an adjacent flash memory cell; and the p-type doped well is located between adjacent control gates corresponding to the drain, the operating method comprising:

applying a high voltage to the p-type doped well, while maintaining the wordline in a ground state, and the bitline and the common source in a floating state, thereby performing an erase operation;

applying a high voltage on the wordline while applying a voltage lower than the wordline voltage to the bitline voltage, and maintaining the voltage of the common source and the p-type doped well voltage in the ground state, thereby performing a programming operation; and

applying a proper voltage to the wordline while applying a voltage lower than the wordline voltage to the bitline, thereby performing a read operation.

22. The operating method of claim 21 for erasing, programming and reading data on the flash memory, wherein the p-type doped well voltage is about 20V when the ease operation is performed.

23. The operating method of claim 21 for erasing, programming and reading data on the flash memory, wherein when the programming operation is performed, the wordline voltage is between 10V and 12V, and the bitline voltage is between 5V and 6.5V.

24. The operating method of claim 21 to erase, programming

and reading data on the flash memory, wherein when the read operation is performed, the wordline voltage is about 3.3V, and the bitline voltage is about 1.5V.